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RESPONSE AFTER-FINAL
EXPEDITED PROCEDURE
EXAMINING GROUP 1765

AF/1765 #8/13 12/24/02

TO THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

TAKENO

Attorney Docket No: 107242-00024

Application No. 09/926,202

Group Art Unit: 1765

Filed: September 24, 2001

Examiner: M. Anderson

For: MANUFACTURING PROCESS FOR SILICON EPITAXIAL WAFER

AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116

Commissioner for Patents
Washington, D.C. 20231

December 19, 2002

Sir:

In reply to the Office Action dated October 4, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claim 6 as follows:

6. (Amended) A manufacturing process for a silicon epitaxial wafer comprising the steps of:

forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from $4 \times 10^{17}/cm^3$ to $10 \times 10^{17}/cm^3$ at a temperature of 1000° C or higher to obtain a silicon epitaxial wafer; and

B1

applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C;

thereby forming new oxygen precipitation nuclei and increasing bulk defect density, without reducing internal gettering.